

EE 435

Lecture 14

Two-Stage Op Amp Design

- Architectures
- Compensation
 - First-stage compensation
 - Load compensated
 - Miller Compensation

Cascaded Amplifier Summary

$$A = \frac{A_0 \tilde{p}}{s + \tilde{p}} \quad \tilde{p}_2 = k\tilde{p}_1$$

- Single-stage amplifiers
 - widely used in industry, little or no concern about compensation
- Two amplifier cascades – for separated poles $4\beta A_{0TOT} > k > 2\beta A_{0TOT}$
 - widely used in industry but compensation is essential
 - spread dependent upon β and most stringent for large β
- Three amplifier cascades - for ideally identical stages $8 > \beta A_0^3$
 - seldom used in industry !
- Three amplifier cascades - for separated poles

$$(1 + k_2 + k_3)(k_2 + k_3 + k_2k_3) > \beta A_{0TOT}$$
 - seldom used in industry but starting to appear but compensation essential!
- Four or more amplifier cascades - problems even larger than for three stages
 - seldom used in industry !

Note: Some amplifiers that are termed single-stage amplifiers in many books and papers are actually two-stage amplifiers and some require modest compensation. Some that are termed two-stage amplifiers are actually three-stage amplifiers. These invariably have a very small gain on the first stage and a very large bandwidth. The nomenclature on this summary refers to the number of stages that have reasonably large gain.

Pole approximation methods

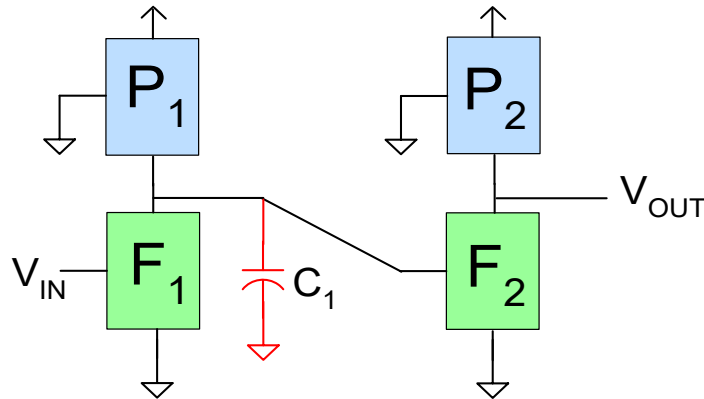
1. Consider all shunt capacitors
2. Decompose these into two sets, those that create low frequency poles and those that create high frequency poles (large capacitors create low frequency poles and small capacitors create high frequency poles)
 $\{C_{L1}, \dots, C_{Lk}\}$ and $\{C_{H1}, \dots, C_{Hm}\}$
3. To find the k low frequency poles, replace all independent voltage sources with ss shorts and all independent current sources with ss opens, all high-frequency capacitors with ss open circuits and, one at a time, select C_{Lh} and determine the impedance facing it, say R_{Lh} if all other low-frequency capacitors are replaced with ss short circuits. Then an approximation for the pole corresponding to C_{Lh} is

$$p_{Lh} = -1/(R_{Lh} C_{Lh})$$

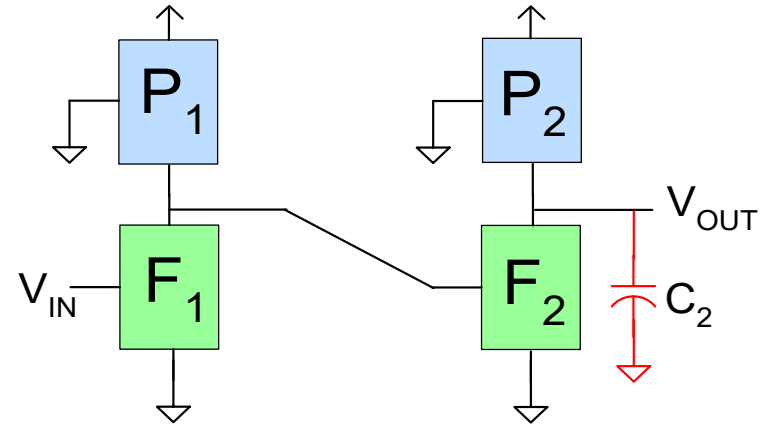
4. To find the m high-frequency poles, replace all independent voltage sources with ss shorts and all independent current sources with ss opens, replace all low-frequency capacitors with ss short circuits and, one at a time, select C_{Hh} and determine the impedance facing it, say R_{Hh} if all other high-frequency capacitors are replaced with ss open circuits. Then the approximation for the pole corresponding to C_{Hh} is

$$p_{Hh} = -1/(R_{Hh} C_{Hh})$$

Compensation of Basic Two-Stage Cascade



Internally Compensated



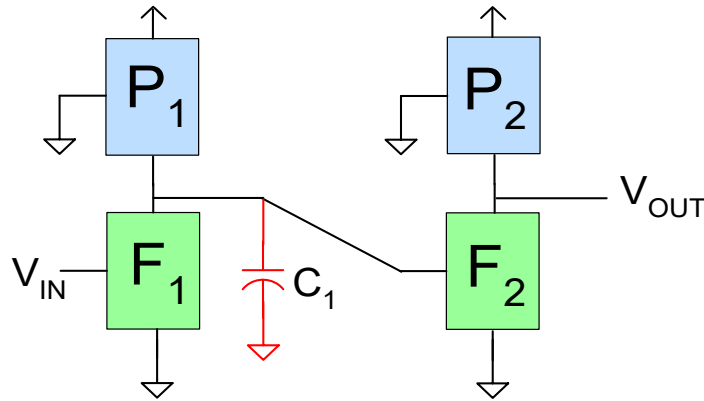
Output Compensated

- Modest variants of the compensation principle are often used
- Internally compensated creates the dominant pole on the internal node
- Output compensated created the dominant pole on the external node
- Output compensated often termed “self-compensated”

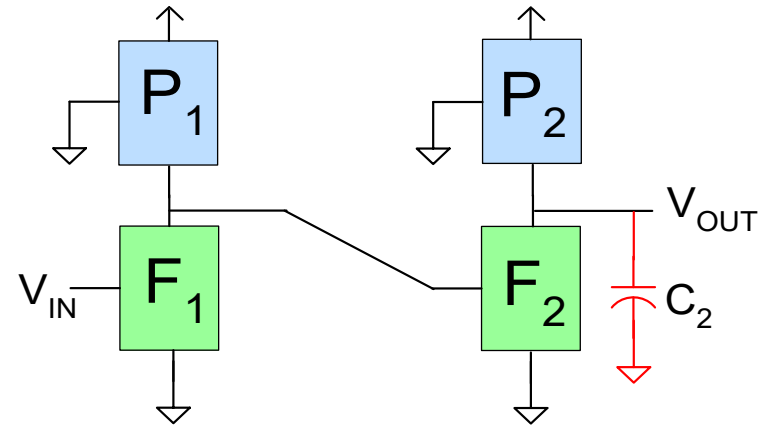
Everything else is just details !!

Compensation of Basic Two-Stage Cascade

(shown for single input, single output but applicable to differential as well)



Internal Node Compensated



Output Compensated

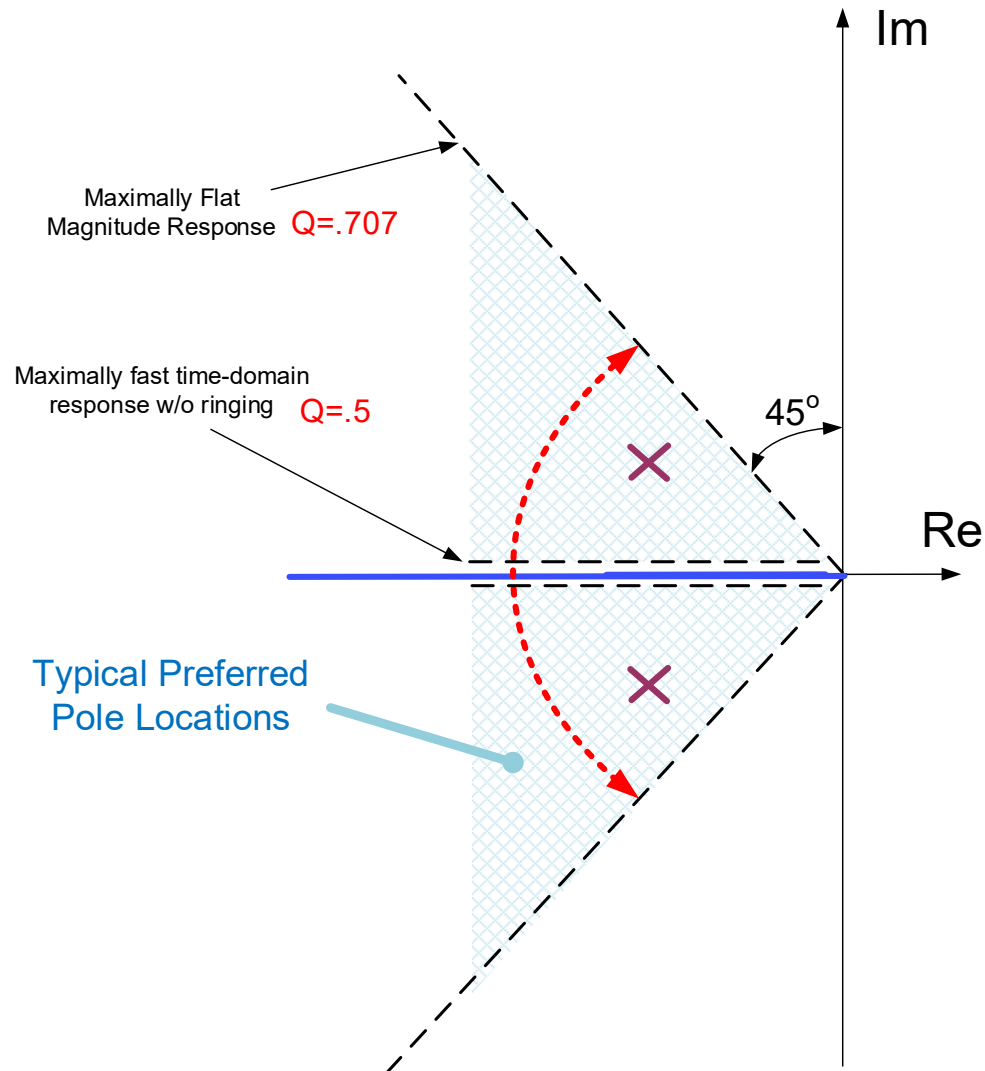
- Modest variants of the compensation principle are often used
- Internal Node compensated creates the dominant pole on the internal node
- Output compensated creates the dominant pole on the external node
- Output compensated often termed “self-compensated”
- Internally Compensated denotes putting compensation circuit on-chip

Everything else is just details !!

Review from Last Time

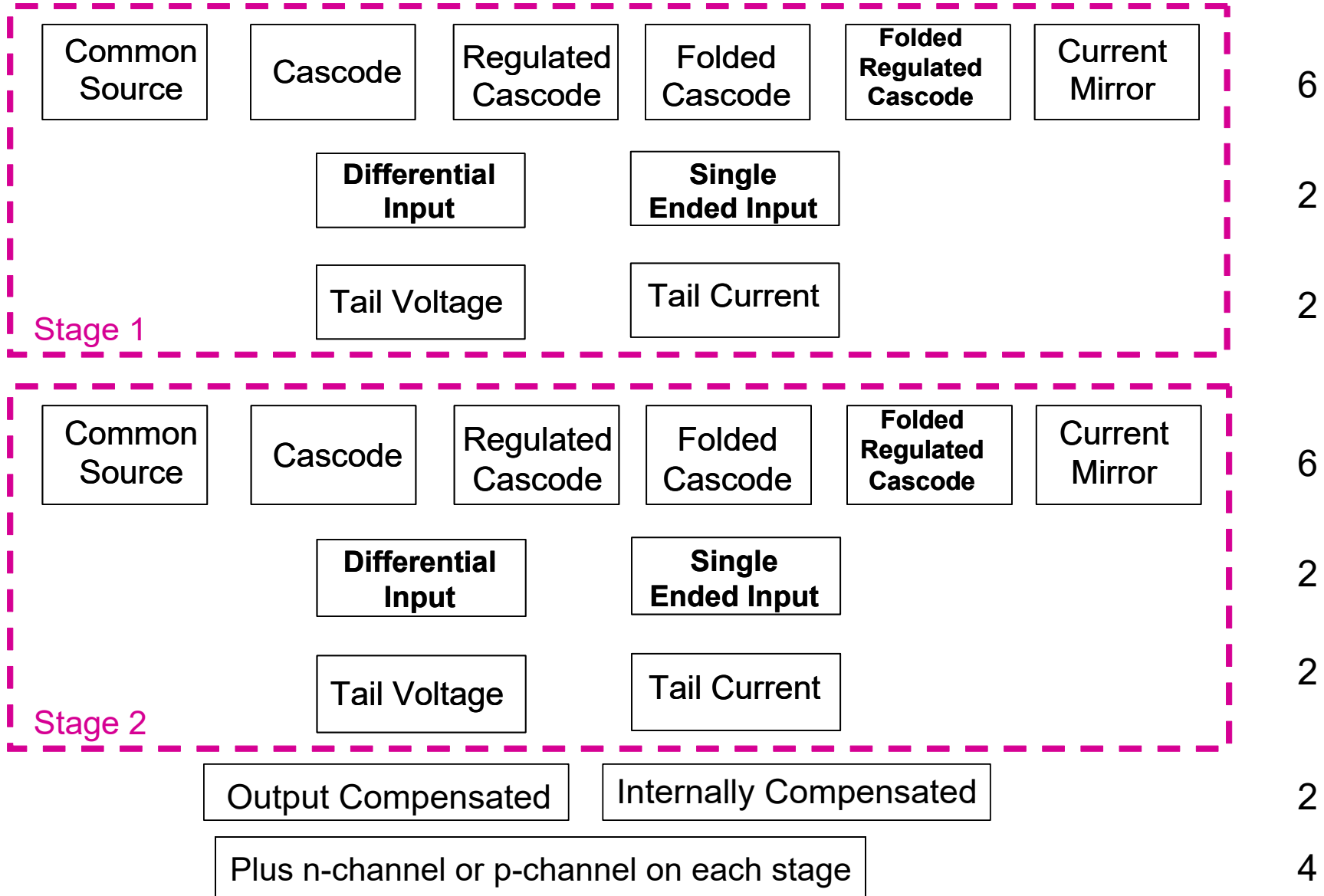
Common Compensation Goal

Typical Target Closed-loop Pole Locations for Feedback Amplifiers



Review from Last Time

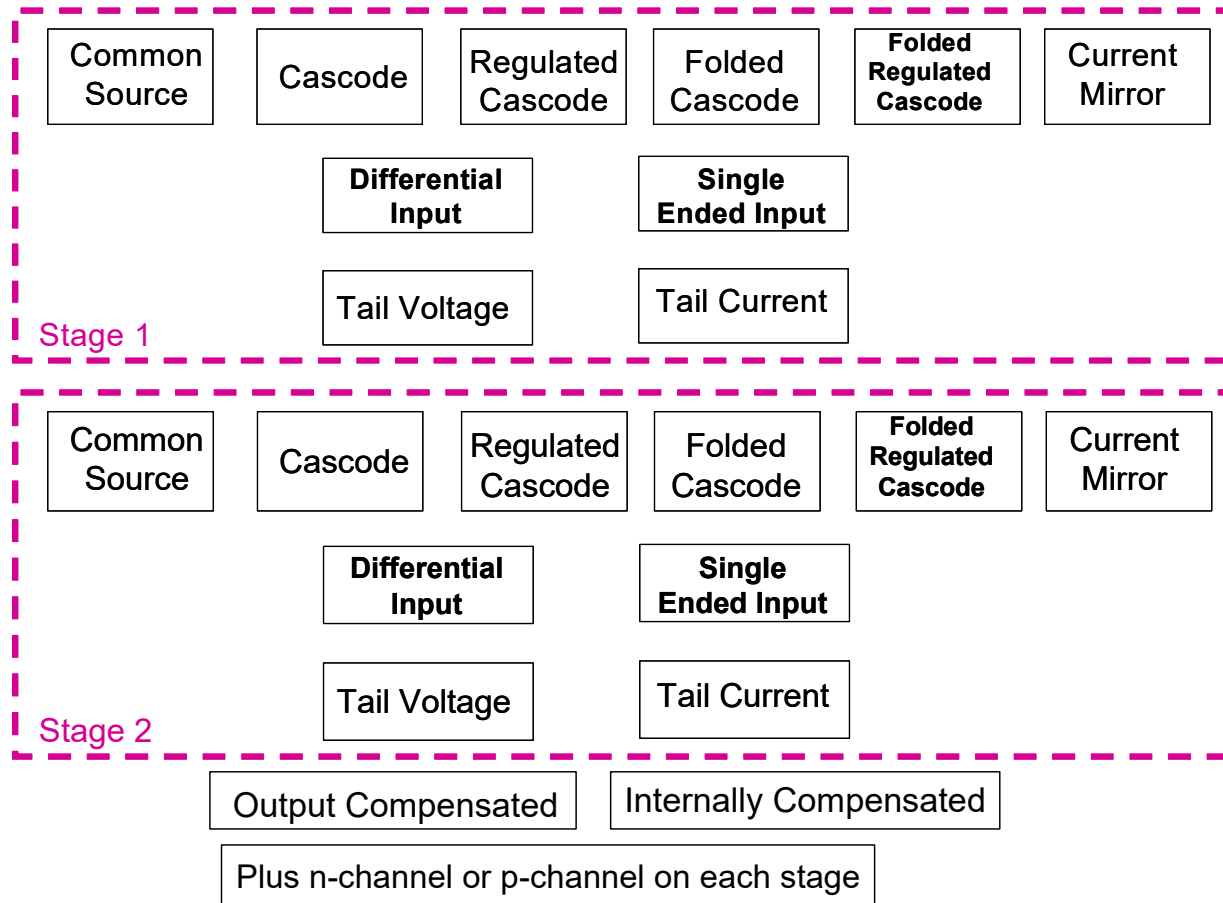
Two-stage Architectural Choices



2304 Choices !!!

Review from Last Time

Two-stage Architectural Choices



Which of these 2304 choices can be used to build a good op amp?

All of them !!

Two-stage Architectural Choices

There are actually a few additional variants so the number of choices is larger

Basic analysis of all is about the same and can be obtained from the quarter circuit of each stage

A very small number of these are actually used

Some rules can be established that provide guidance as to which structure may be most useful in a given application

Two-stage Architectural Choices

Guidelines for Architectural Choices

Tail current source usually used in first stage, tail voltage source in second stage

Large gain usually used in first stage, smaller gain in second stage

First and second stage usually use quarter circuits of opposite types (n-p or p-n)

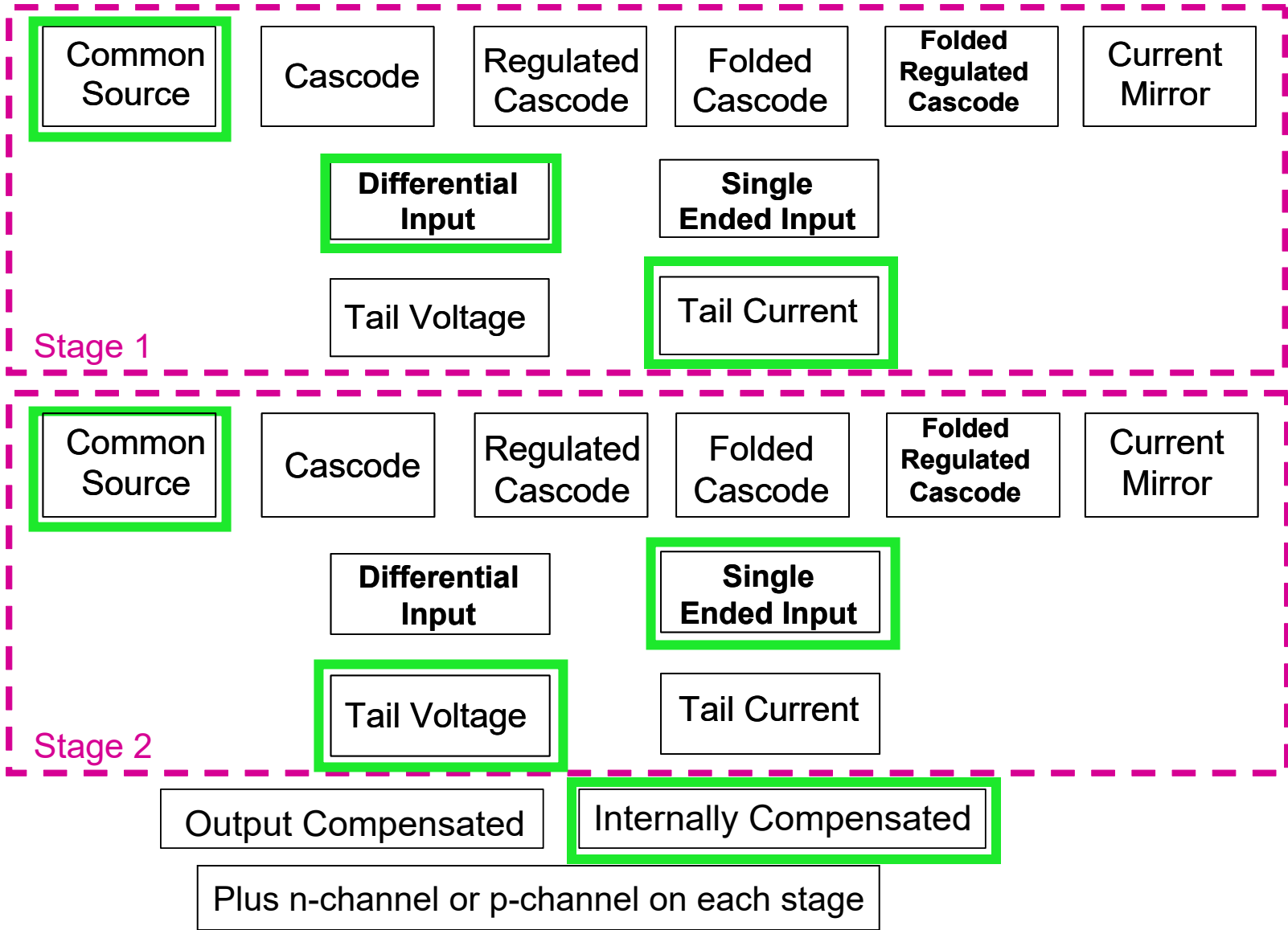
Input common mode input range of concern on first stage but output swing of first stage of reduced concern. Output range on second stage of concern.

CMRR of first stage of concern but not of second stage

Noise on first stage of concern but not of much concern on second stage

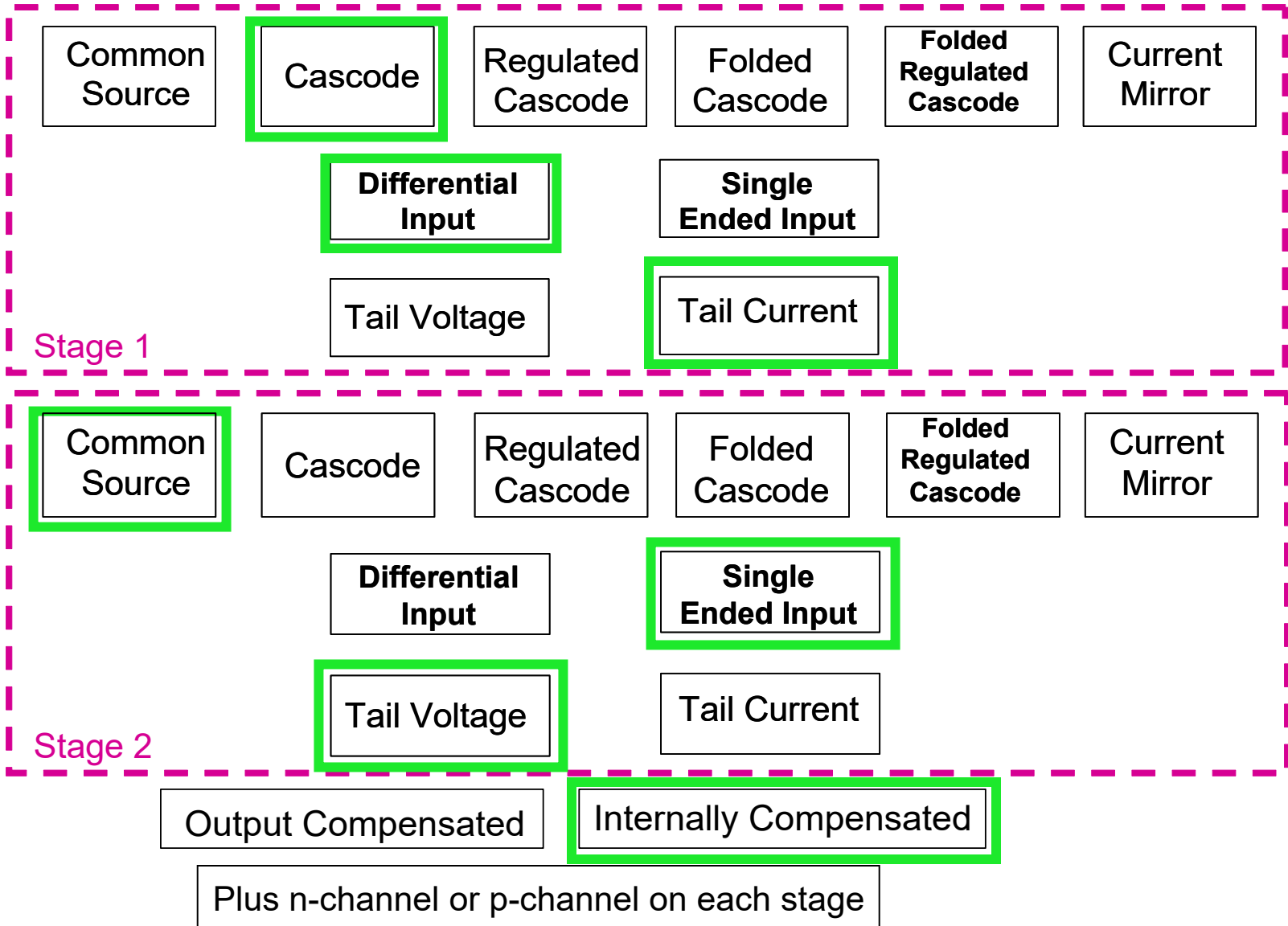
Offset voltage usually dominated by that of the first stage

Two-stage Architectural Choices



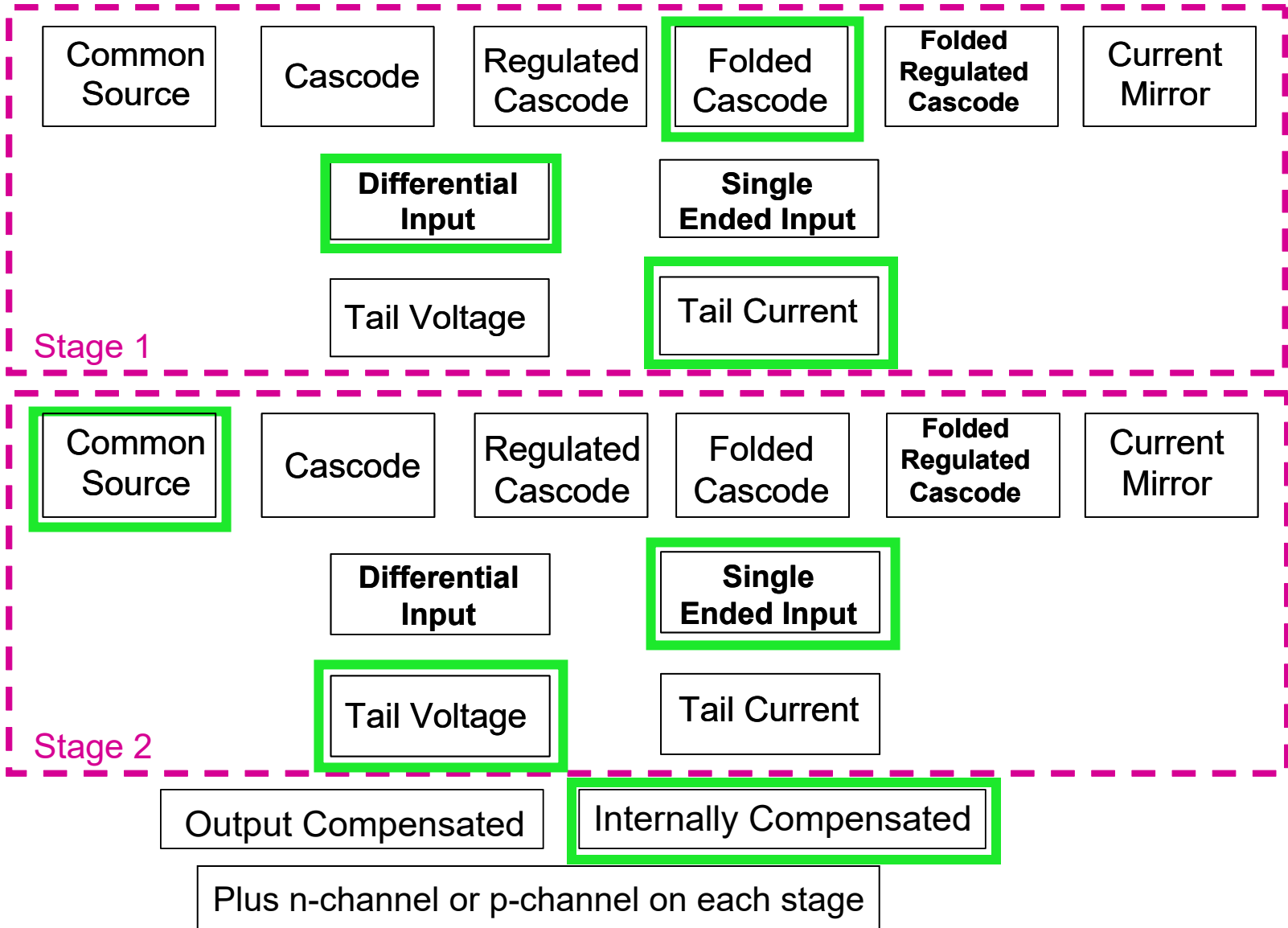
Basic Two-Stage Op Amp

Two-stage Architectural Choices



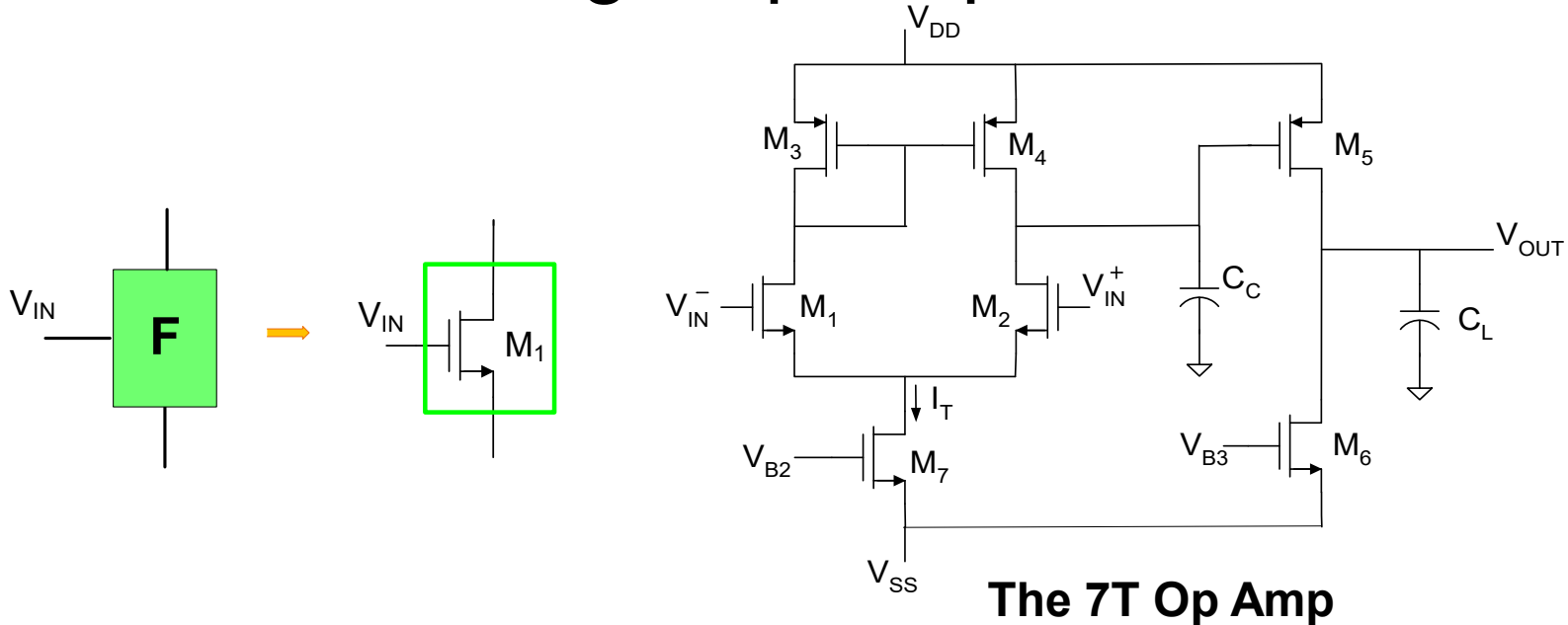
Cascode-Cascade Two-Stage Op Amp

Two-stage Architectural Choices



Folded Cascode-Cascode Two-Stage Op Amp

Basic Two-Stage Op Amp (compensated on first stage)

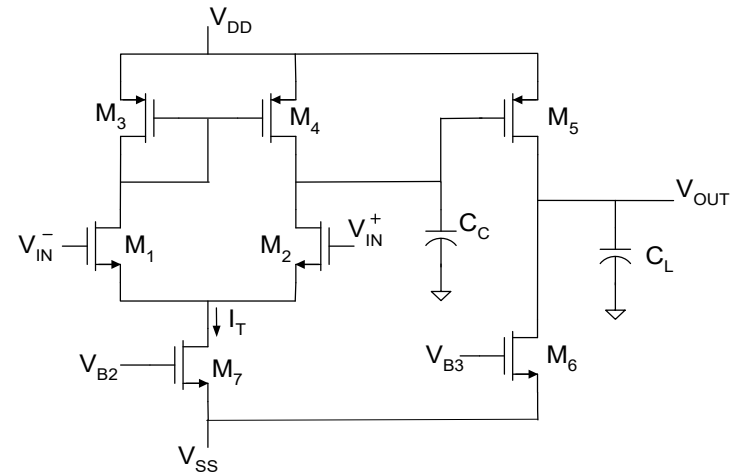


- o One of the most widely used op amp architectures
- o Essentially just a cascade of two common-source stages
- o Compensation Capacitor C_C used to get wide pole separation
- o Pole on drain node of M_1 usually of little concern
- o Two poles in differential operation of amplifier usually dominate performance
- o C_C can be internal (termed internally compensated) or external (termed externally compensated)
- o External compensation works but is usually not practical
- o No universally accepted strategy for designing this seemingly simple amplifier

Pole spread $k \beta A_{01} A_{02}$ $2 < k < 4$ makes C_C unacceptably large for on-chip solutions

Basic Two-Stage Op Amp

The 7T Op Amp



Pole spread $\propto \beta A_{01} A_{02}$ makes C_C unacceptably large

- Remember, pole spread strongly dependent upon β
- Large β (i.e. $\beta=1$) requires large C_C
- C_C is usually an additional capacitor that is added
- Concept of Miller compensation will be used to reduce actual size of C_C

What about just making C_C larger than what is needed?

GB will degrade, power and area will increase

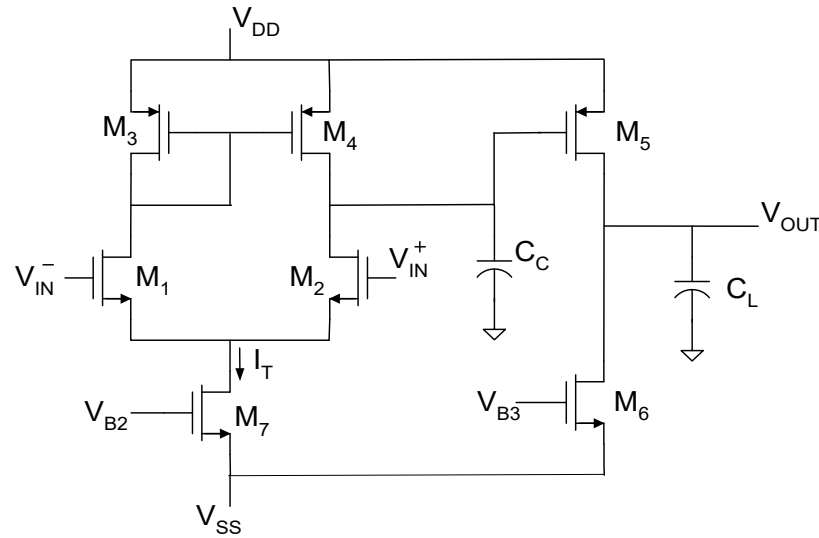
What about providing additional compensation by making C_L larger too?

Poles will move together and degrade performance

What about compensating for worst-case $\beta=1$ so β dependence can be ignored?

- Good solution for catalog parts so application space large but at a cost !
- Penalty in GB, power, and area severe if compensated for much different β than needed

Basic Two-Stage Op Amp



Pole spread $\propto \beta A_{01} A_{02}$ makes C_C unacceptably large

Important to compensate just for what is needed, even a little more comes at a rather big penalty in performance, power, or area !!

Selected Commercial Op Amps



LF147, LF347-N

www.ti.com

SNOSBH1D –MAY 1999–REVISED MARCH 2013

LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

Check for Samples: [LF147](#), [LF347-N](#)

FEATURES

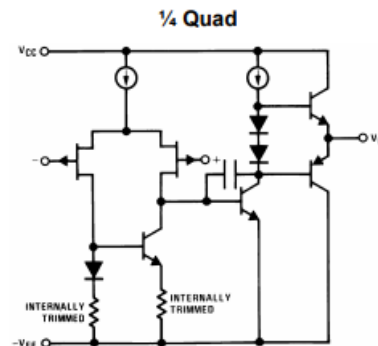
- Internally Trimmed Offset Voltage: 5 mV max
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 7.2 mA
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: $\leq 0.02\%$
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

DESCRIPTION

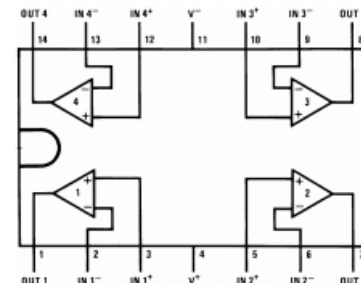
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Simplified Schematic



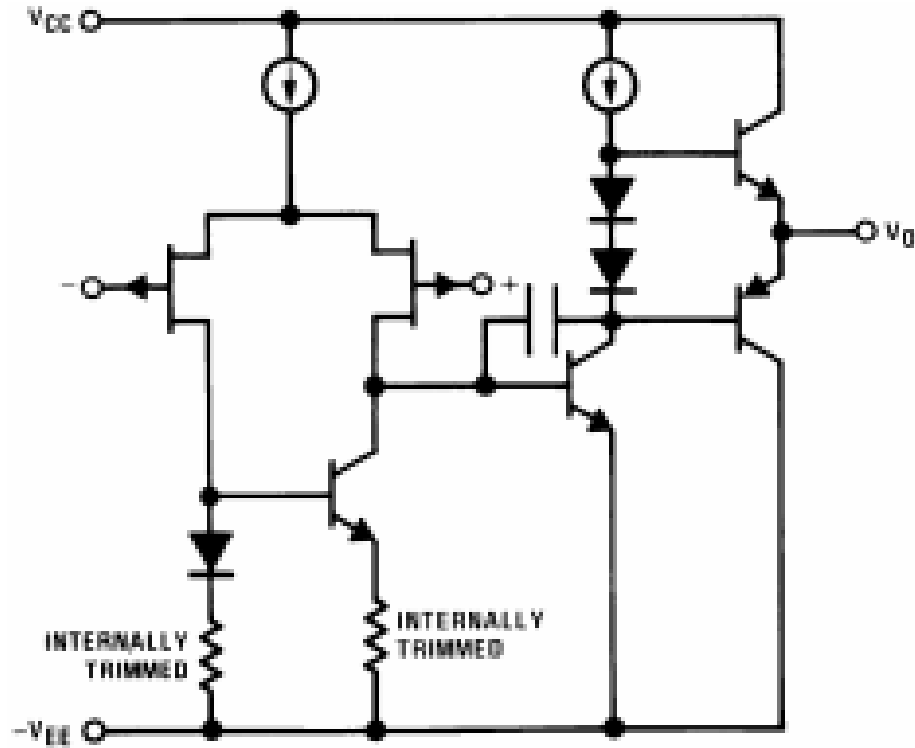
Connection Diagram



LF147 available as per JM38510/11906.

Figure 1. 14-Pin PDIP / CDIP / SOIC

Selected Commercial Op Amps



Selected Commercial Op Amps



LM224K, LM224KA, LM324, LM324A, LM324K, LM324KA, LM2902
LM124, LM124A, LM224, LM224A, LM2902V, LM2902K, LM2902KV, LM2902KAV

SLOS066W – SEPTEMBER 1975 – REVISED MARCH 2015

LMx24, LMx24x, LMx24xx, LM2902, LM2902x, LM2902xx, LM2902xxx Quadruple Operational Amplifiers

1 Features

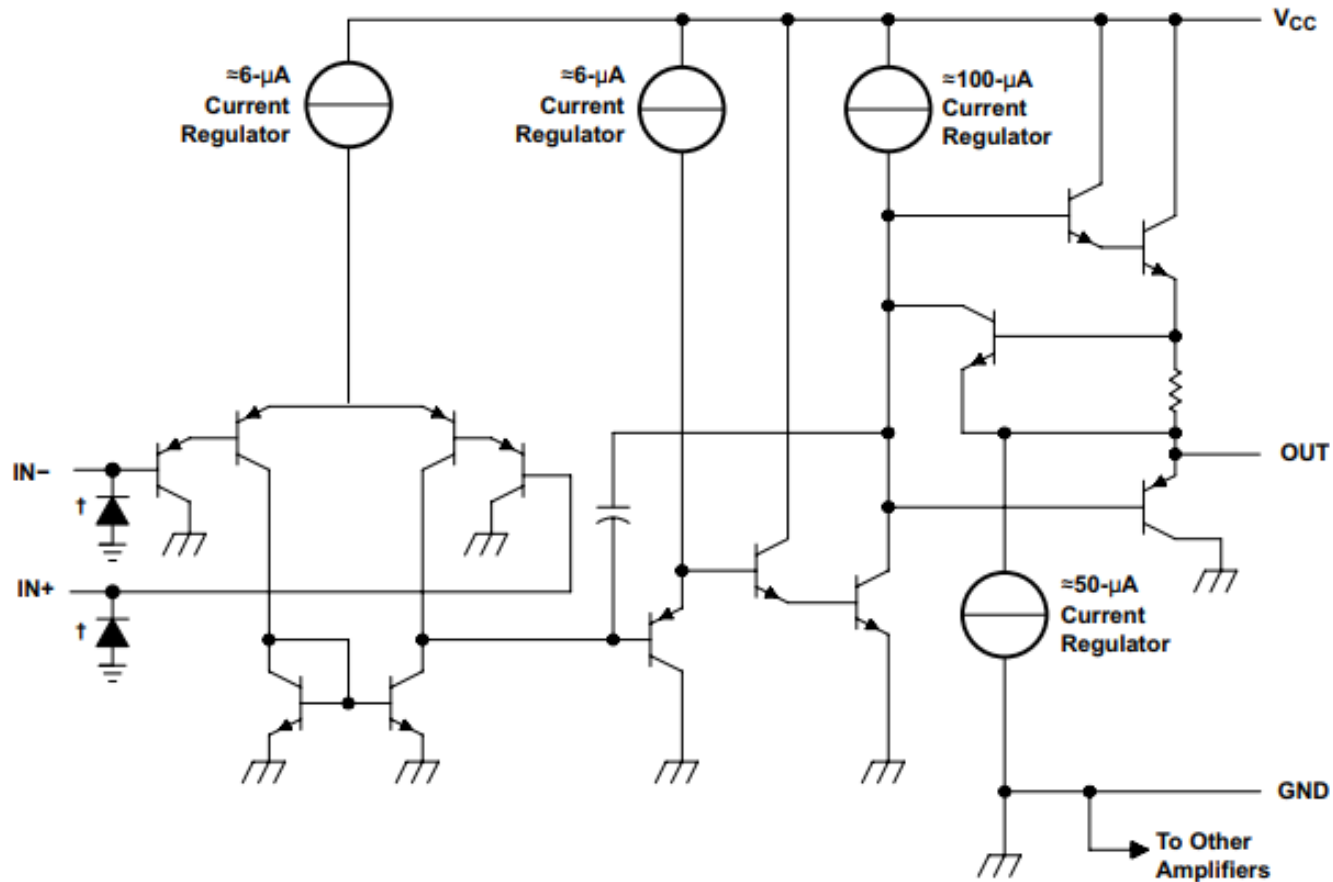
- 2-kV ESD Protection for:
 - LM224K, LM224KA
 - LM324K, LM324KA
 - LM2902K, LM2902KV, LM2902KAV
- Wide Supply Ranges
 - Single Supply: 3 V to 32 V (26 V for LM2902)
 - Dual Supplies: ± 1.5 V to ± 16 V (± 13 V for LM2902)
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA Typical
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
 - Input Offset Voltage: 3 mV Typical

2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorders and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

Selected Commercial Op Amps

8.2 Functional Block Diagram



Voltage Feedback Op Amp Gain and Bandwidth

INTRODUCTION

This tutorial examines the common ways to specify op amp gain and bandwidth. It should be noted that this discussion applies to voltage feedback (VFB) op amps—current feedback (CFB) op amps are discussed in a later tutorial ([MT-034](#)).

OPEN-LOOP GAIN

Unlike the ideal op amp, a practical op amp has a finite gain. The open-loop dc gain (usually referred to as A_{VOL}) is the gain of the amplifier without the feedback loop being closed, hence the name “open-loop.” For a precision op amp this gain can be vary high, on the order of 160 dB (100 million) or more. This gain is flat from dc to what is referred to as the *dominant pole corner frequency*. From there the gain falls off at 6 dB/octave (20 dB/decade). An octave is a doubling in frequency and a decade is $\times 10$ in frequency). If the op amp has a single pole, the open-loop gain will continue to fall at this rate as shown in Figure 1A. A practical op amp will have more than one pole as shown in Figure 1B. The second pole will double the rate at which the open-loop gain falls to 12 dB/octave (40 dB/decade). If the open-loop gain has dropped below 0 dB (unity gain) before it reaches the frequency of the second pole, the op amp will be unconditionally stable at any gain. This will be typically referred to as *unity gain stable* on the data sheet. If the second pole is reached while the closed-loop gain is greater than 1 (0 db), then the amplifier may not be stable. Some op amps are designed to be stable only at higher closed-loop gains, and these are referred to as *decompensated* op amps.

Selected Commercial Op Amps

Decompensated Op Amp



30 V, High Speed, Low Noise, Low Bias Current, JFET Operational Amplifier

Data Sheet

ADA4627-1/ADA4637-1

FEATURES

Low offset voltage: 200 μV maximum

Offset drift: 1 $\mu\text{V}/^\circ\text{C}$ typical

Very low input bias current: 5 pA maximum

Extended temperature range: -40°C to $+125^\circ\text{C}$

$\pm 5\text{ V}$ to $\pm 15\text{ V}$ dual supply

ADA4627-1 GBW: 19 MHz

ADA4637-1 GBW: 79 MHz

Voltage noise: 6.1 nV/ $\sqrt{\text{Hz}}$ at 1 kHz

ADA4627-1 slew rate: 82 V/ μs

ADA4637-1 slew rate: 170 V/ μs

High gain: 120 dB typical

High CMRR: 116 dB typical

High PSRR: 112 dB typical

APPLICATIONS

High impedance sensors

Photodiode amplifier

Precision instrumentation

Phase-locked loop filters

High end, professional audio

DAC output amplifier

ATE

Medical

PIN CONFIGURATIONS

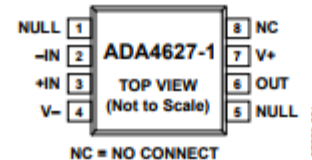


Figure 1. 8-Lead SOIC_N (R-8)

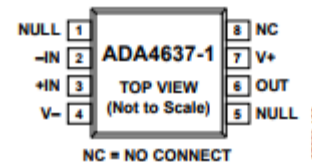
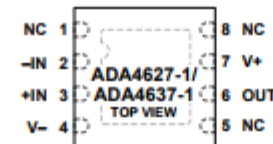


Figure 2. 8-Lead SOIC_N (R-8)



NOTES

1. NC = NO CONNECT.
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V-.

Figure 3. 8-Lead LFCSP_VD (CP-8-13)

Selected Commercial Op Amps

ADA4627-1/ADA4637-1

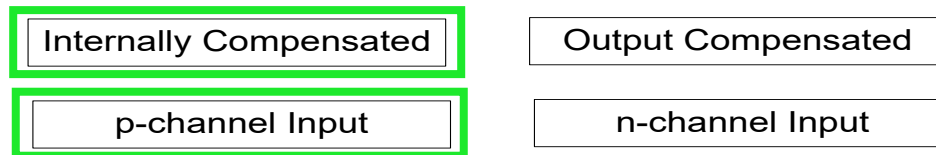
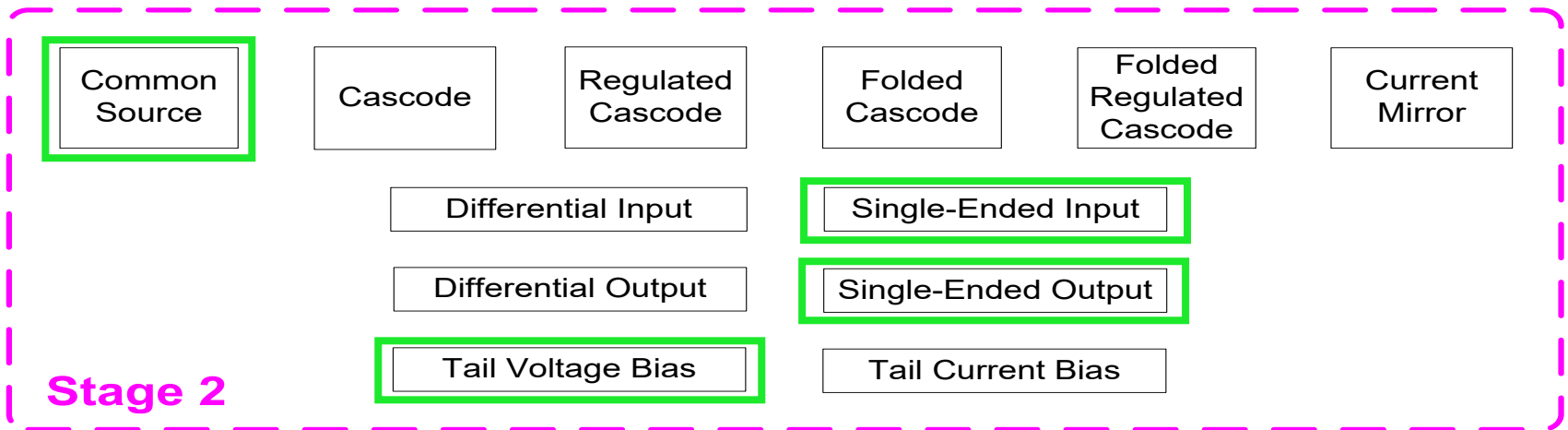
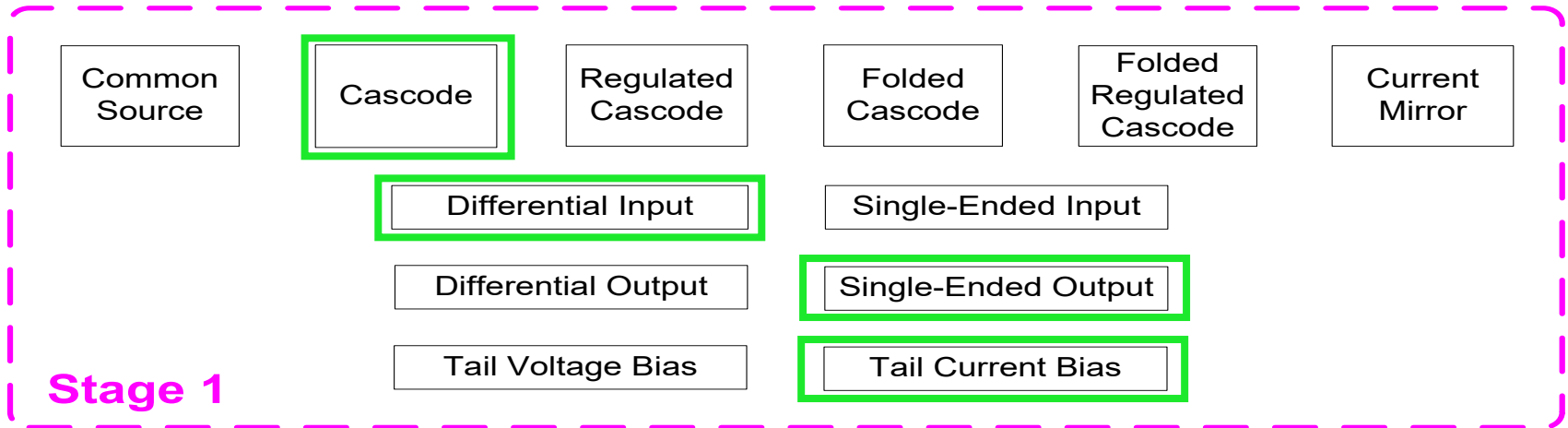
Data Sheet

| Parameter | Symbol | Test Conditions/Comments | B Grade | | | A Grade | | | Unit |
|---|----------|---|---------|----------|-----|----------|-----|---------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Settling Time to 0.01% ADA4627-1 | t_s | $V_{IN} = 10\text{ V step}, C_L = 35\text{ pF}, R_L = +1\text{ k}\Omega, A_V = -1$ | | 550 | | 550 | | ns | |
| ADA4637-1 | | $V_{IN} = 10\text{ V step}, C_L = 35\text{ pF}, R_L = +1\text{ k}\Omega, A_V = -4$ | | 300 | | 300 | | ns | |
| Settling Time to 0.1% ADA4627-1 | t_s | $V_{IN} = 10\text{ V step}, C_L = 35\text{ pF}, R_L = +1\text{ k}\Omega, A_V = -1$ | | 450 | | 450 | | ns | |
| ADA4637-1 | | $V_{OUT} = 10\text{ V step}, C_L = 35\text{ pF}, R_L = +1\text{ k}\Omega, A_V = -4$ | | 200 | | 200 | | ns | |
| Gain Bandwidth Product ADA4627-1 | GBP | $R_L = 1\text{ k}\Omega, C_L = 20\text{ pF}, A_V = 1$ | 16^4 | 19 | | 16^4 | 19 | MHz | |
| ADA4637-1 | | $A_V = 10$ | | 79.9 | | 79.9 | | | |
| Phase Margin ADA4627-1 | Φ_M | $R_L = 1\text{ k}\Omega, C_L = 20\text{ pF}, A_V = 1$ | | 72 | | 72 | | Degrees | |
| ADA4637-1 | | $A_V = 10$ | | 85 | | 85 | | | |
| Total Harmonic Distortion + Noise | THD + N | $V_{IN} = 6\text{ V rms}, f = 1\text{ kHz}, A_V = 1,$ ADA4627-1 | | 0.000045 | | 0.000045 | | % | |

Example:

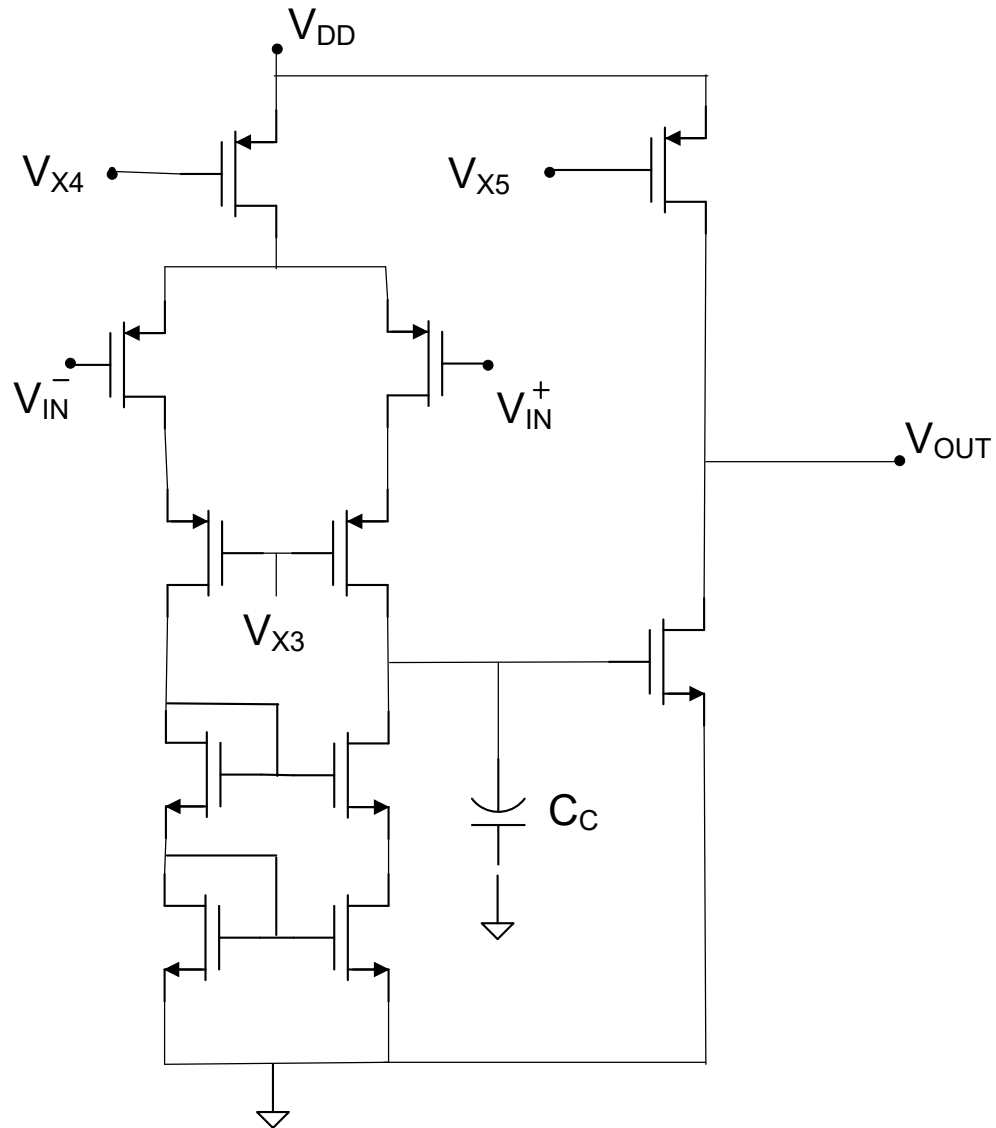
Sketch the circuit of a two-stage internally compensated op amp with a telescopic cascode first stage, single-ended output, tail current bias first stage, tail voltage bias second stage, p-channel inputs and n-channel inputs on the second stage.

Two-stage Architectural Choices



Cascode-Cascode Two-Stage Op Amp

Example Solution



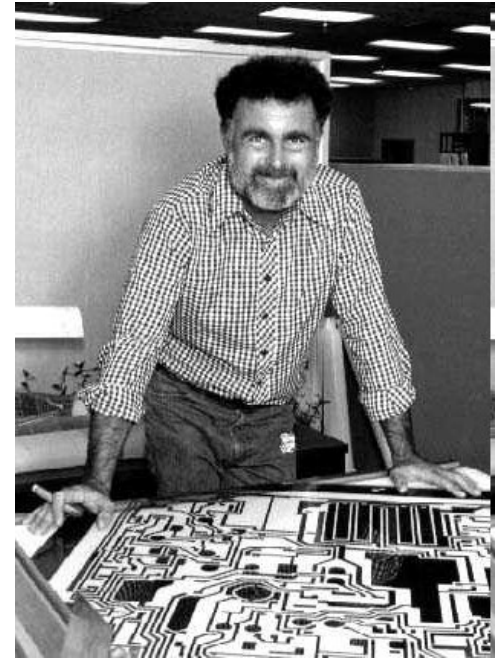
First Commercial Operational Amplifier



K2-W Op Amp by Philbrick, 1952-1971

Inventor of the Two-Stage Op Amp

Robert Widlar

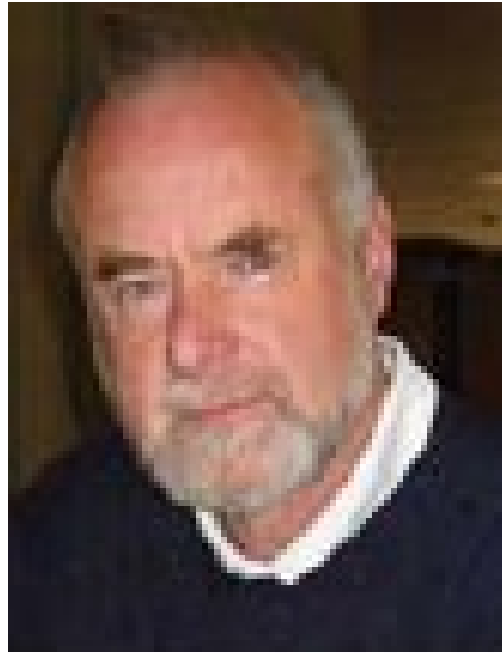


Many say he started the field of analog IC design, considered a brilliant engineer

“Widlar began his career at Fairchild semiconductor, where he designed a couple of pioneering op amps. By 1966, the commercial success of his designs became apparent, and Widlar asked for a raise. He was turned down, and jumped ship to the fledgling National Semiconductor. At National he continued to turn out amazing designs, and was able to retire just before his 30th birthday in 1970.”
(from posted www site)

Inventor of the internally-compensated Op Amp

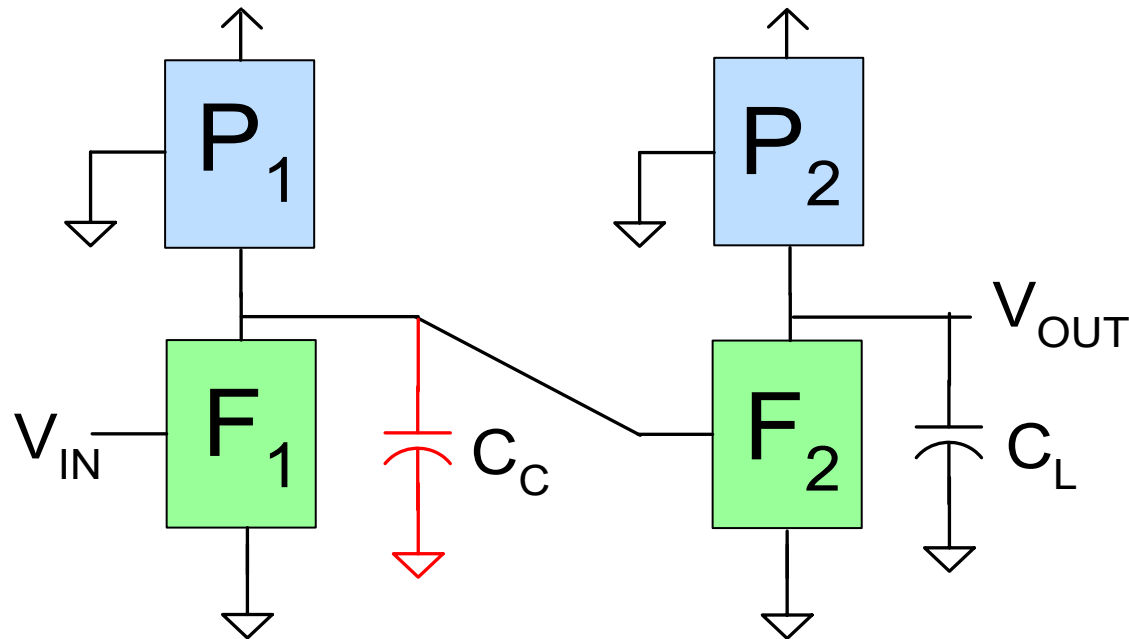
Dave Fullagar



(from posted www site)

- Designed the first internally-compensated (C_C on chip) op amp, the 741
- Fullagar was 26 years old when this was designed (introduced?)
- Introduced in 1968
- Largest selling integrated circuit ever
- Still in high-volume production even though over 50 years old
- Fullagar later started the linear design activities at Intersil
- Cofounder (catalyst) of Maxim

Analysis of Internal Node Compensated Two-Stage Op Amps



p_1 pole on first stage, p_2 pole on second stage

Consider single-ended input-output (differential analysis only slightly different)

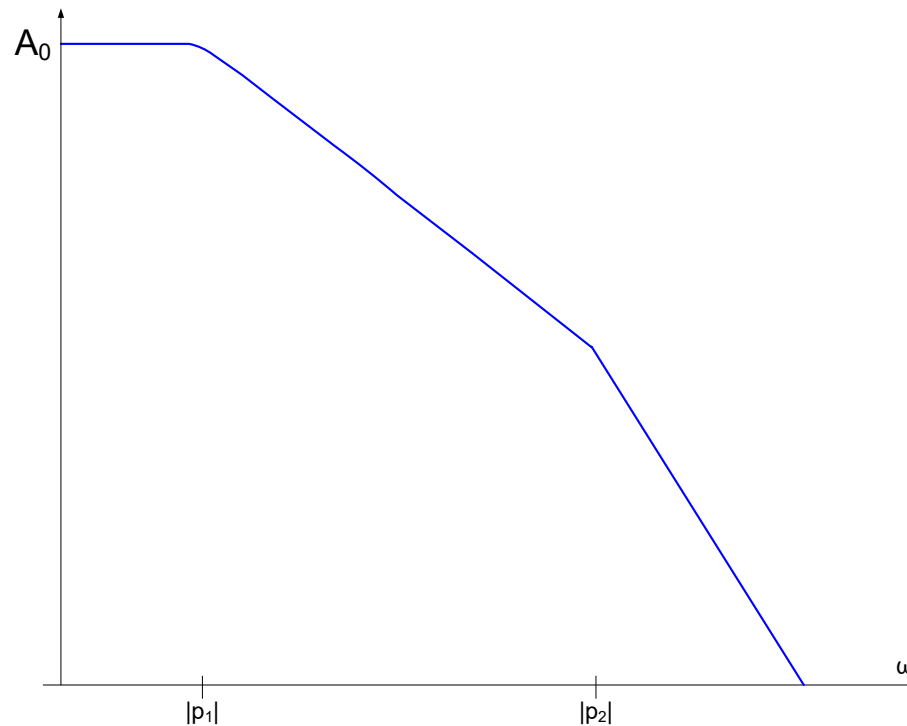
Can't get everything but can get most of the small-signal results

Since internal node compensated, must have $p_1 \ll p_2$

Analysis of Intern Node Compensated Two-Stage Op Amps

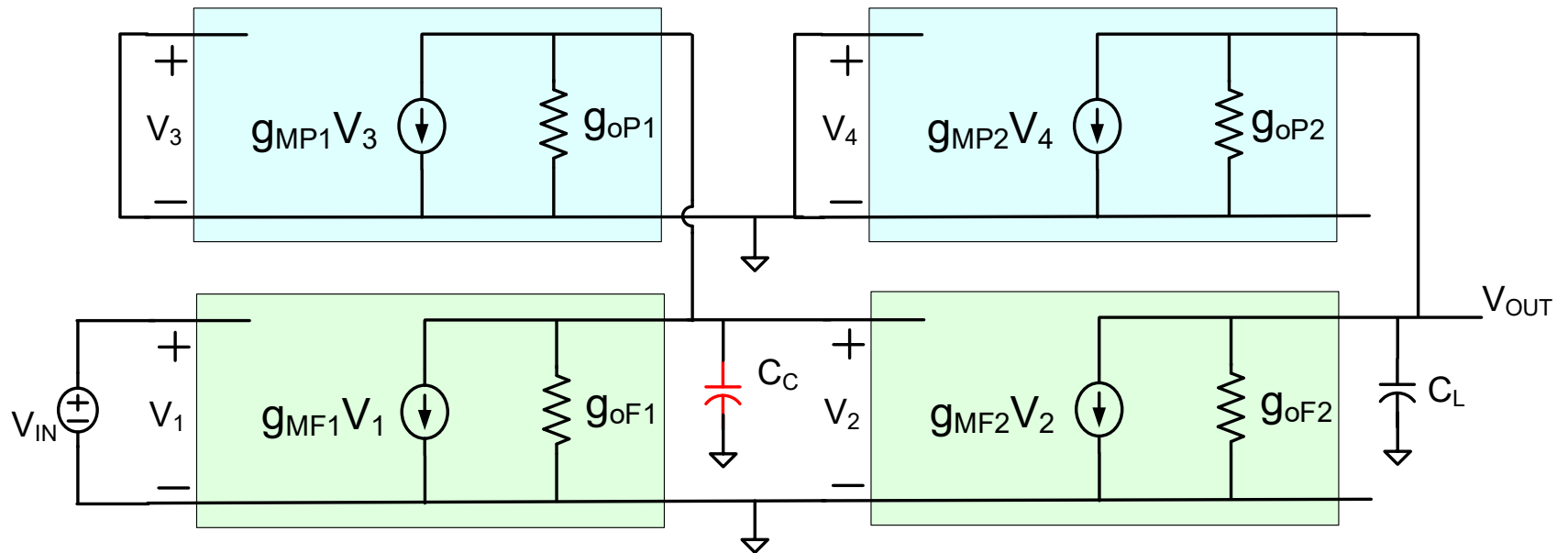
$$A(s) = \frac{A_0}{\left(\frac{s}{|p_1|} + 1\right)\left(\frac{s}{|p_2|} + 1\right)}$$

For $|p_1| \ll |p_2|$

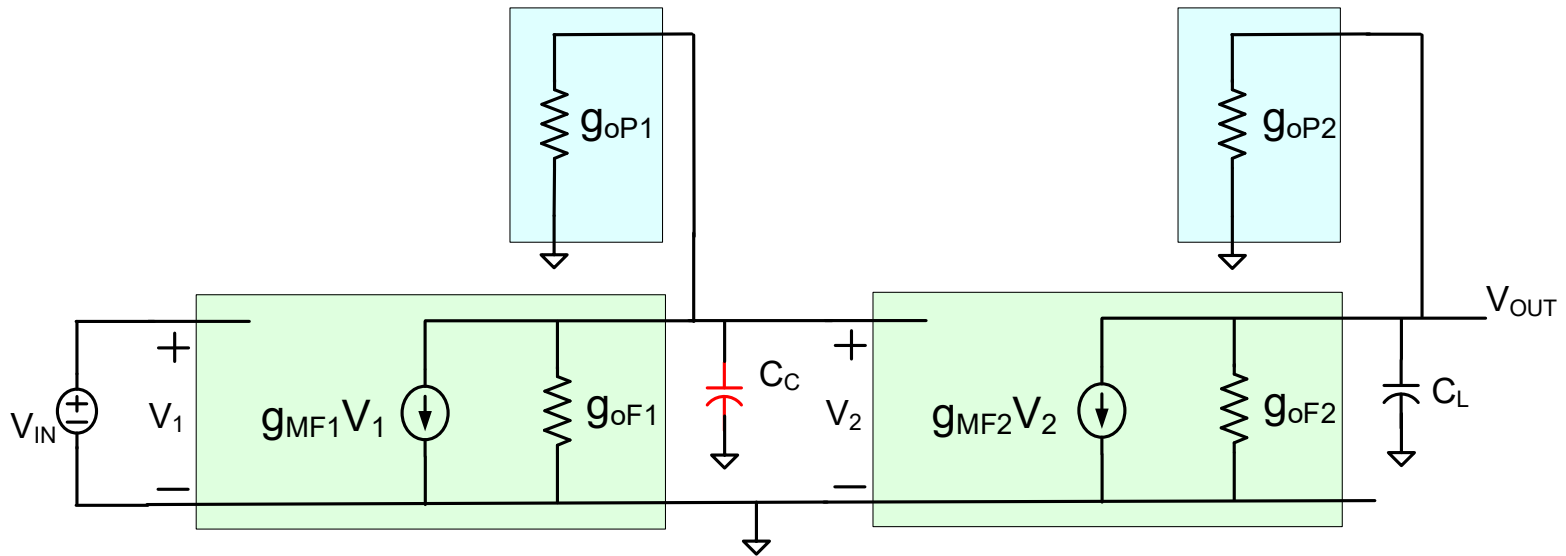


$$BW \approx |p_1|$$

Analysis of Intern Node Compensated Two-Stage Op Amps



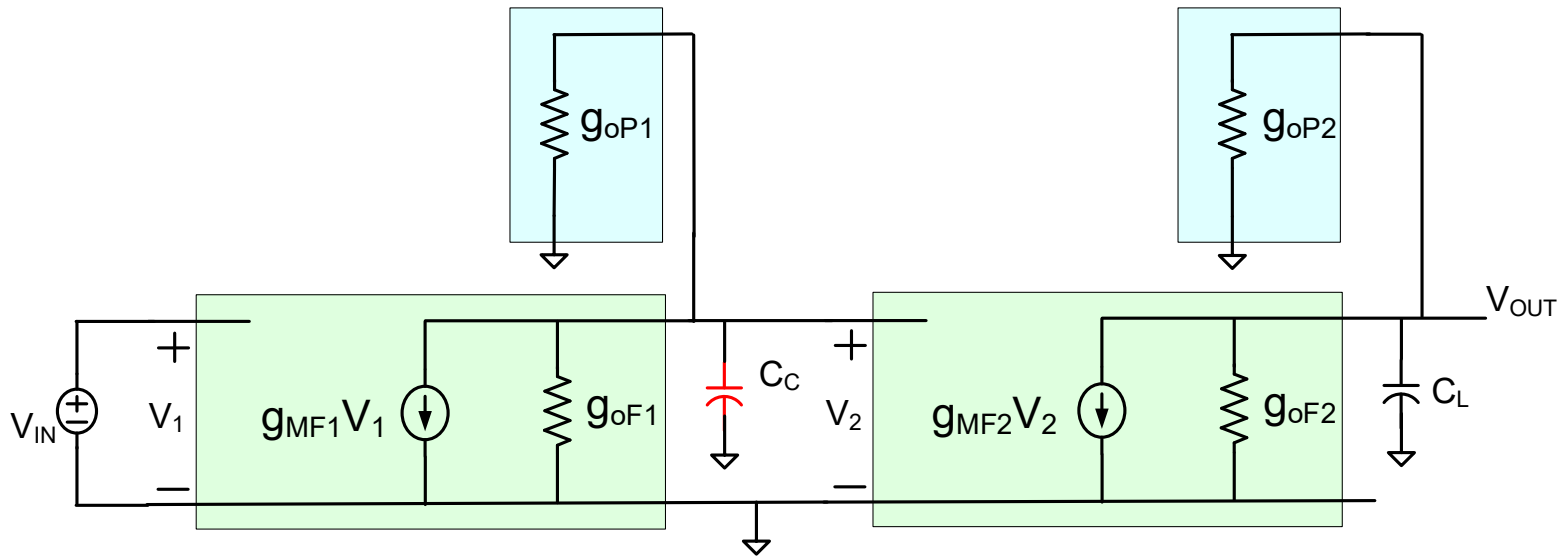
Analysis of Internal Node Compensated Two-Stage Op Amps



$$\left. \begin{aligned} V_2 (sC_C + g_{oF1} + g_{oP1}) + g_{mF1} V_{IN} &= 0 \\ V_{OUT} (sC_L + g_{oP2} + g_{oF2}) + g_{mF2} V_2 &= 0 \end{aligned} \right\}$$

$$A_V(s) = \frac{-g_{mF1}}{sC_C + g_{oF1} + g_{oP1}} \cdot \frac{-g_{mF2}}{sC_L + g_{oP2} + g_{oF2}}$$

Analysis of Internal Node Compensated Two-Stage Op Amps



$$A_{V0} = \left(\frac{g_{mF1}}{g_{oF1} + g_{oP1}} \right) \left(\frac{g_{mF2}}{g_{oF2} + g_{oP2}} \right)$$

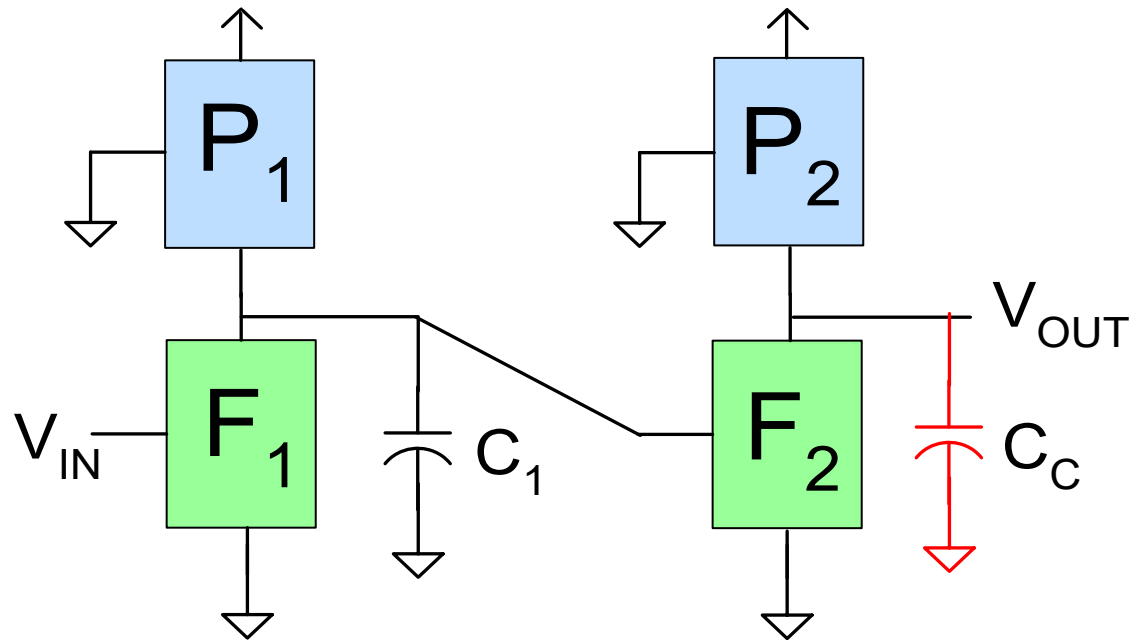
$$|p_2| = \frac{(g_{oF2} + g_{oP2})}{C_L}$$

$$|p_1| = \frac{(g_{oF1} + g_{oP1})}{C_C}$$

$$BW = |p_1|$$

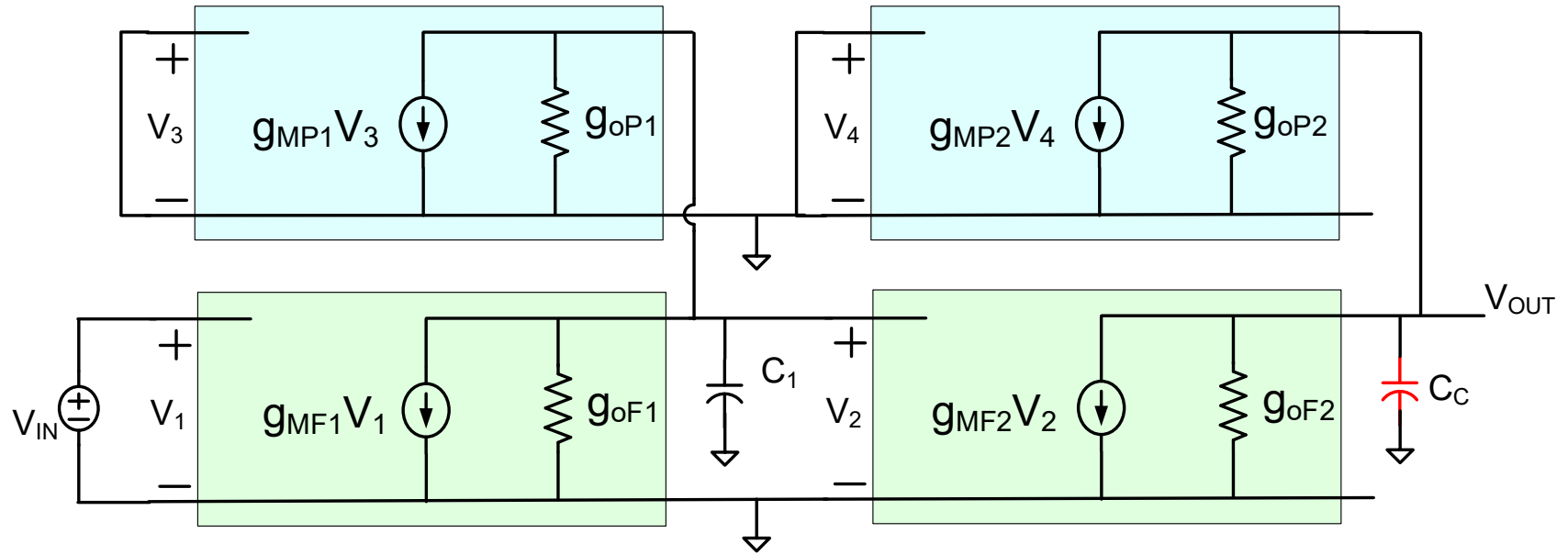
$$GB = \frac{g_{mF1} g_{mF2}}{(g_{oF2} + g_{oP2}) C_C}$$

Analysis of Load Compensated Two-Stage Op Amps

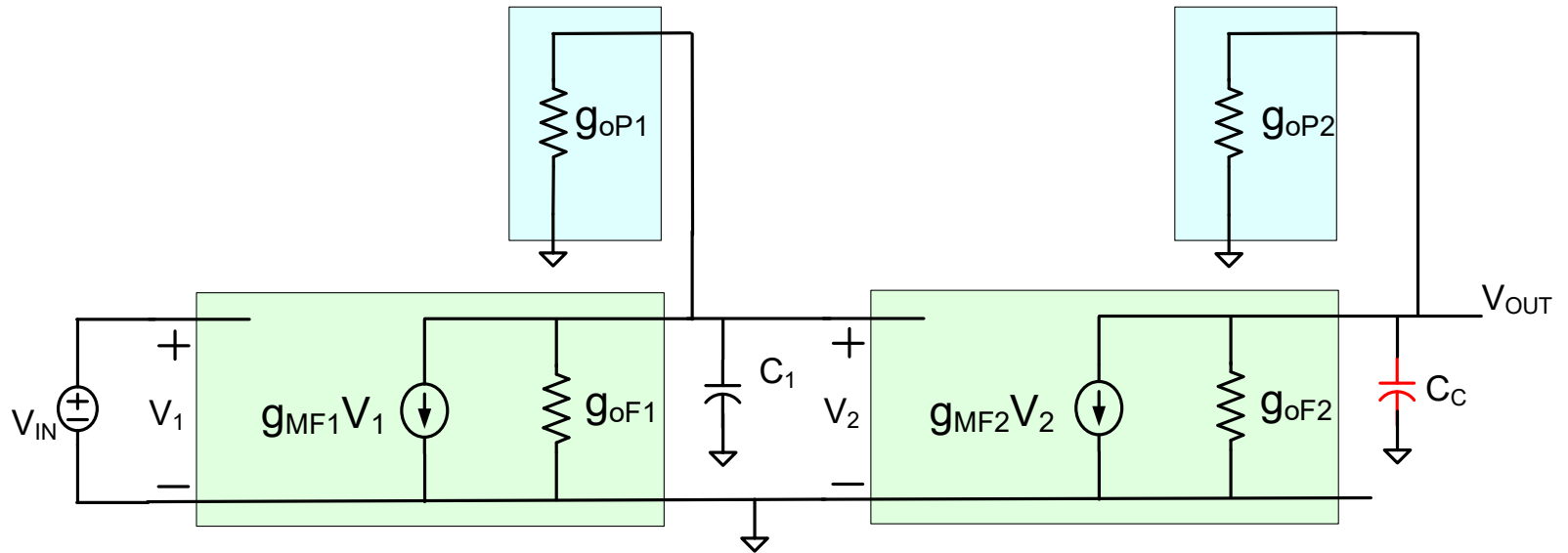


Can't get everything but can get most of the small-signal results

Analysis of Load Compensated Two-Stage Op Amps



Analysis of Externally Compensated Two-Stage Op Amps



$$A_{V0} = \left(\frac{g_{mF1}}{g_{oF1} + g_{oP1}} \right) \left(\frac{g_{mF2}}{g_{oF2} + g_{oP2}} \right)$$

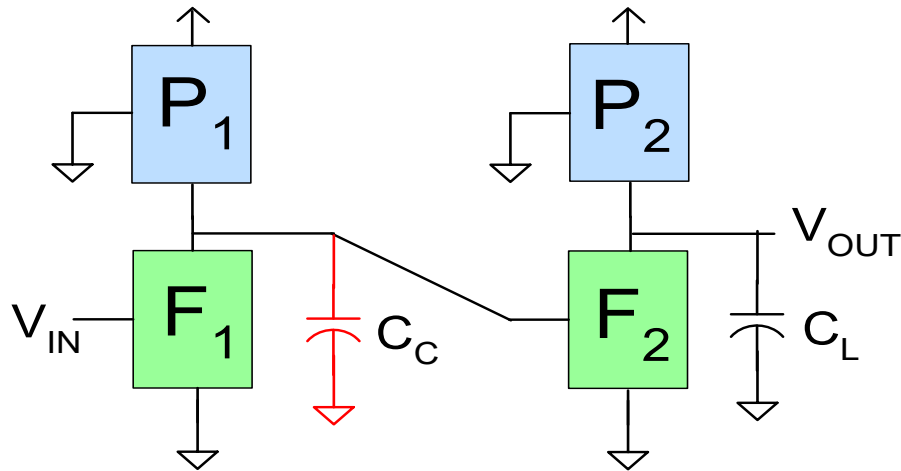
$$|p_2| = \frac{(g_{oF2} + g_{oP2})}{C_C}$$

$$|p_1| = \frac{(g_{oF1} + g_{oP1})}{C_1}$$

$$BW = |p_2|$$

$$GB = \frac{g_{mF1}g_{mF2}}{(g_{oF1} + g_{oP1})C_C}$$

Consider Again the Internal-Node Compensated Two-Stage Op Amp



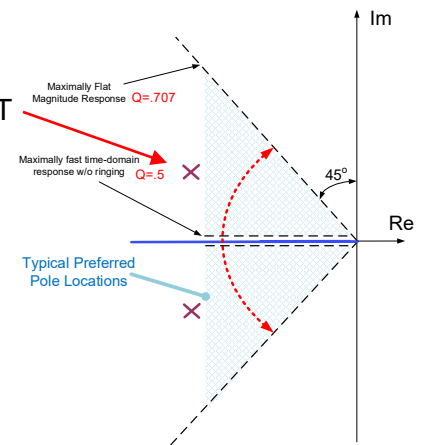
Recall approximate compensation requirements: $4\beta A_{0TOT} > k > 2\beta A_{0TOT}$

where $|p_2| = k|p_1|$

Thus, approximately, $3\beta A_{0TOT} = \frac{|p_2|}{|p_1|}$ $k \cong 3\beta A_{0TOT}$

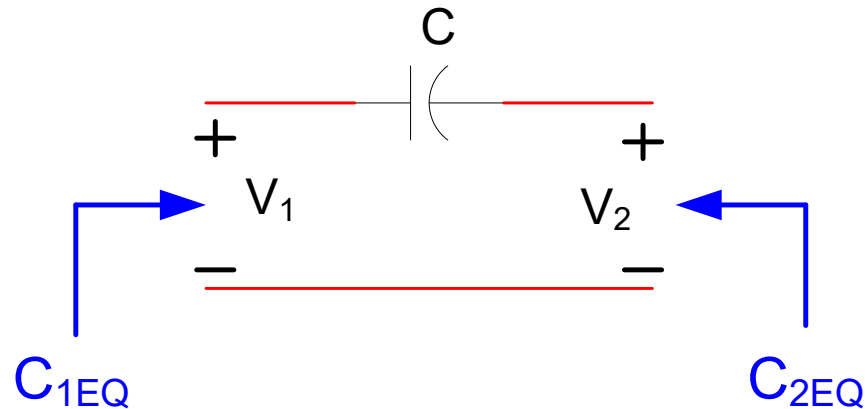
$$3\beta \left(\frac{g_{mF1}}{g_{oF1} + g_{oP1}} \right) \left(\frac{g_{mF2}}{g_{oF2} + g_{oP2}} \right) \approx \left(\frac{g_{oF2} + g_{oP2}}{C_L} \right) \left(\frac{C_C}{g_{oF1} + g_{oP1}} \right)$$

$$C_C \approx \left(3\beta \frac{g_{mF1} g_{mF2}}{(g_{oF2} + g_{oP2})^2} \right) C_L$$



Since the pole ratio needs to be very large, C_C gets very large !

Miller Capacitance - Review



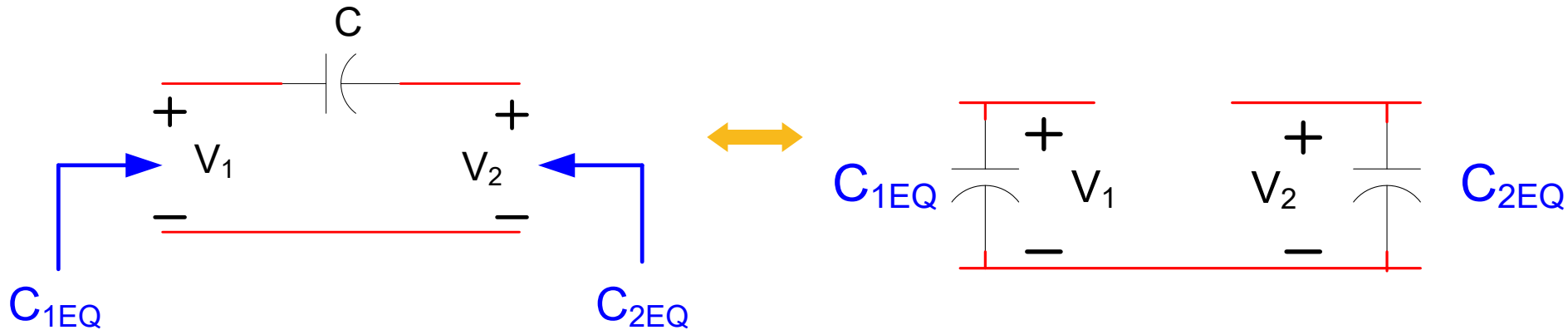
If $V_2 = -AV_1$ then for A large

$$C_{1EQ} = C(1 + A) \approx CA \quad C_{2EQ} = C\left(1 + \frac{1}{A}\right) \approx C$$

Thus, a large effective capacitance can be created with a much smaller capacitor if a capacitor bridges two nodes with a large inverting gain !!

Note: The symbol "A" used in the Miller Capacitance should not be confused with the gain of the op amp

Miller Capacitance - Review



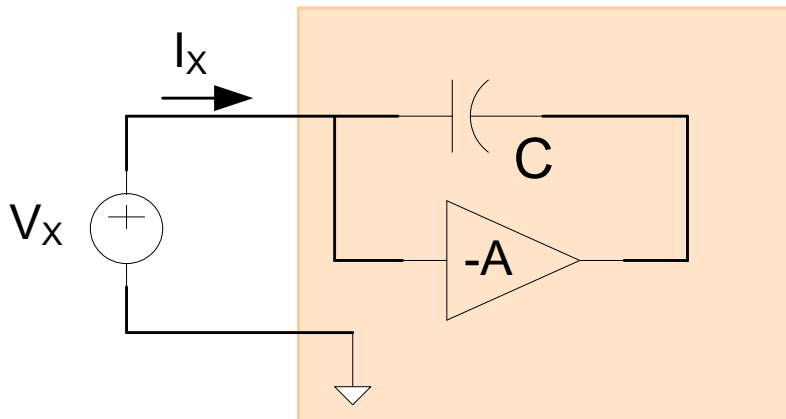
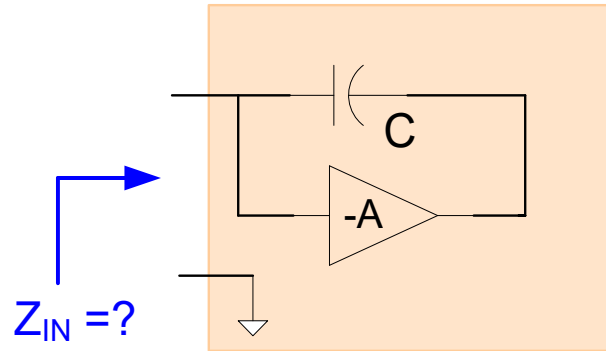
If $V_2 = -AV_1$ then for A large

$$C_{1EQ} = C(1 + A) \approx CA \qquad C_{2EQ} = C\left(1 + \frac{1}{A}\right) \approx C$$

- If A changes with frequency, C_{1EQ} and C_{2EQ} are no longer pure capacitors
- More useful for giving a concept than for accurate actual analysis because of frequency dependence of A

Miller Capacitance - Review

The Basic Concept – from capacitance multiplication



$$I_X = [V_X - (-AV_X)]sC = V_X s [C(1+A)]$$

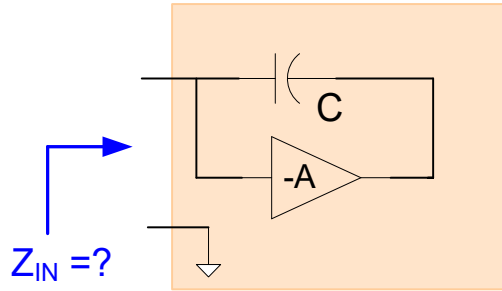
thus

$$Z_{IN} = \frac{V_X}{I_X} = \frac{1}{s [C(1+A)]}$$

So, if A is constant, input looks like a capacitor of value

$$C_{EQ} = C(1+A)$$

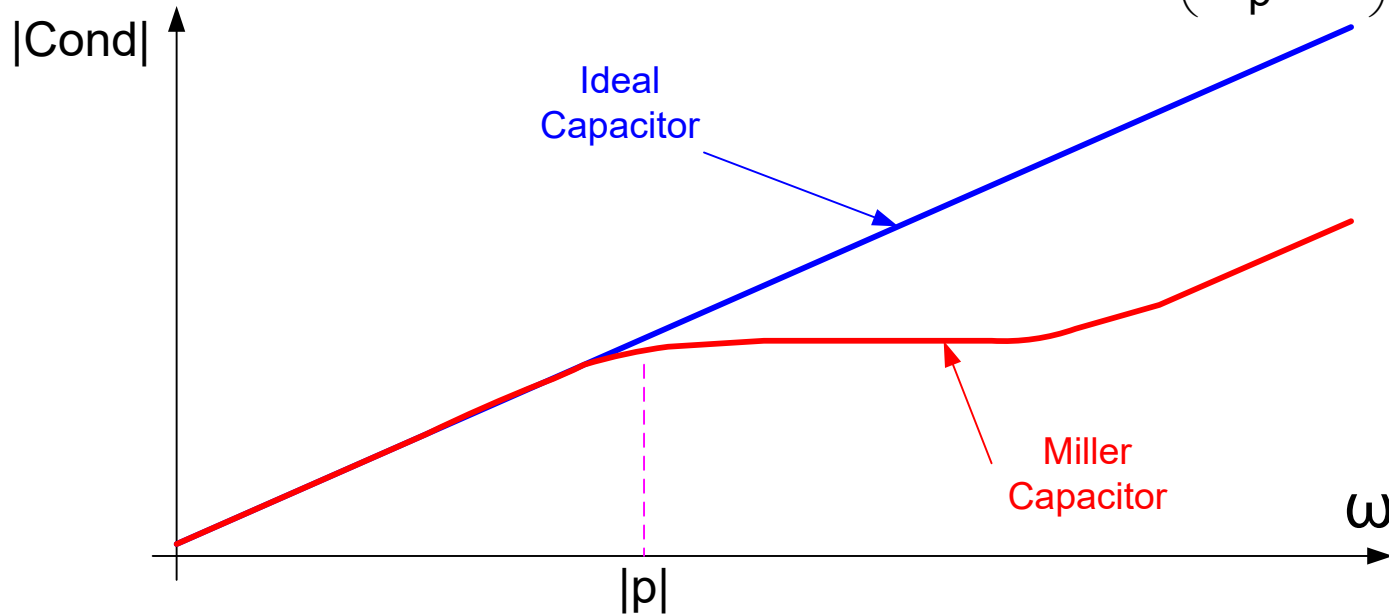
Miller Capacitance - Review



$$Z_{IN} = \frac{V_X}{I_X} = \frac{1}{s[C(1+A)]}$$

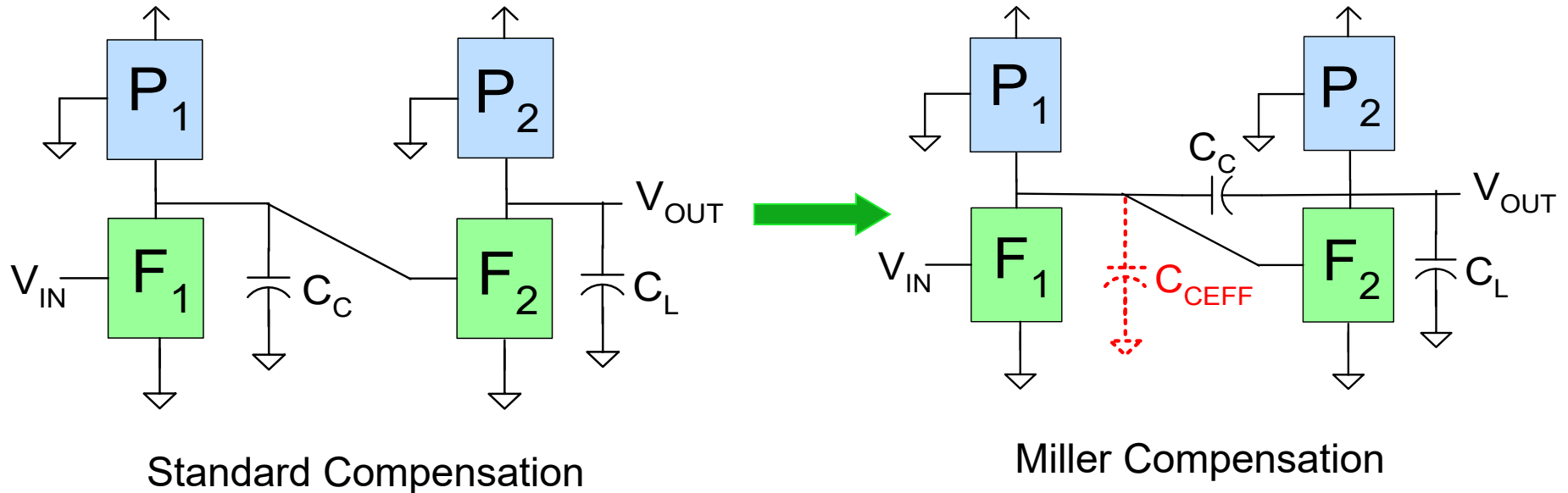
$$\text{If } A(s) = \frac{A_0}{\frac{s}{p} + 1}$$

$$G_{IN} = s[C(1+A)] = sC \left(\frac{\frac{s}{p} + 1 + A_0}{\frac{s}{p} + 1} \right)$$



Does not behave as a capacitor for $\omega > p$

Internal-Node Miller-Compensated Two-Stage Op Amp



The second stage amplifier can be used to create a Miller capacitance at its input with no circuit overhead!

Compensation capacitance reduced by approximately the gain of the second stage! (the value of the two C_C 's are not the same)

Since the gain of the second stage is not constant, however, a new analysis is needed

If C_C is small enough, this becomes an internally compensated op amp with internal-node compensation



Stay Safe and Stay Healthy !

End of Lecture 14